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EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,039	PAPADOPOULOU ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-15,17-24 and 26-31* is/are rejected.

7)☒ Claim(s) *3, 6, 16 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/708,039, amendment filed 5/17/2007. Claim 3 has been amended. Claims 1-31 are pending in this application.

2. Applicant's arguments filed 5/17/2007 have been fully considered but they are not persuasive. The applicable rejections from the previous office action are incorporated herein.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-2, 4-5, 7-15, 17-24 and 26-31 are rejected under 35 U.S.C. 102(e)** as being anticipated by Ikeda (US PG Pub 2004/0096092).

5. With respect to claims 1, 12 and 21, Ikeda teaches:

partitioning (dividing image into Voronoi regions so that each region includes single pattern edge, see Fig 33, S83 and Figure 16) an edge (see edge of shape in Figure 16) of a shape (see Figure 11, IC shape edge is divided into sections [i.e. intervals]) in the IC design into a plurality of intervals (lattice sections, see Description of Figures 9-12, paragraphs [0119]-[0122]); and

assigning at least one dimension to each interval (length [i.e. dimension] is imparted to each edge of the lattice [i.e. interval], paragraph [0170]).

6. With respect to claim 30, Ikeda teaches:

means for partitioning (dividing image into Voronoi regions so that each region includes single pattern edge) an edge of a shape (see Figure 11, IC shape edge is divided into sections [i.e. intervals]) in the IC design into a plurality of intervals (lattice sections, see Description of Figures 9-12, paragraphs [0119]-[0122]), the partitioning means including:

means for generating a core Voronoi diagram for the shape using a first metric (preparing a voronoi diagram with respect to the extracted partial point sequence, paragraph []0055);

means for partitioning the edge based on the core Voronoi diagram (Voronoi diagram prepared with respect to vertices [i.e. endpoints of each edge interval], paragraph [0121]; also see Voronoi diagram being generated in Figure 11);

means for assigning at least one dimension to each interval (length [i.e. dimension] is imparted to each edge of the lattice [i.e. interval], paragraph [0170]) using a second metric (length metric Lij, see paragraph [0170]); and

means for using the at least one dimension (comparing Voronoi diagrams, which suggests the use of comparing respective lengths, widths or radii, see paragraph [0249]) to evaluate a check rule (checking the edges and vertices that do not match each other, paragraph [0249]).

7. With respect to claims 2, 13 and 22, Ikeda teaches all the elements of claims 1, 12 and 21, from which the claims depend respectively. Ikeda teaches: generating a core Voronoi diagram for the shape (preparing a voronoi diagram, paragraph [0055]); and partitioning the edge based on the core Voronoi diagram (Voronoi diagram prepared with respect to vertices [i.e. endpoints of each edge interval], paragraph [0121]; also see Voronoi diagram being generated in Figure 11).

8. With respect to claims 4, 14 and 23, Ikeda teaches all the elements of claim 2, 13 and 22, from which the claims depend respectively. Ikeda teaches: wherein the partitioning step further includes partitioning the edge based on a core element for each vertex of the core Voronoi diagram (as seen in Fig 11, pattern elements have edges divided by the vertices shown in the Voronoi diagram figure).

9. With respect to claims 5, 15 and 24, Ikeda teaches all the elements of claims 4, 14 and 23, from which the claims depend respectively. Ikeda teaches: wherein the core element is one of a largest possible core element (unit cell [i.e. core element] has a larger size, paragraph [0023]) and a smallest possible core element.

10. With respect to claims 7, 17 and 26, Ikeda teaches all the elements of claims 1, 12 and 22, from which the claims depend respectively. Ikeda teaches: wherein the at least one dimension includes a width for each interval (weight function for each edge o the lattice, paragraph [0170]) and a spacing to a neighboring shape for each interval (a length [i.e. spacing to next shape] for each edge of the lattice [i.e. interval], paragraph [0170]).

11. With respect to claims 8, 18 and 27, Ikeda teaches all the elements of claims 1, 12 and 22, from which the claims depend respectively. Ikeda teaches: wherein the dimension is a function of another dimension (Lij, a length dimension which is a function of two dimensions I and j, see paragraph [0170]).

12. With respect to claims 9, 19 and 28, Ikeda teaches all the elements of claims 1, 12 and 22, from which the claims depend respectively. Ikeda teaches: using the at least one dimension (comparing Voronoi diagrams, which suggests the use of comparing respective lengths, widths or radii, see paragraph [0249]) to evaluate a check rule (checking the edges and vertices that do not match each other, paragraph [0249]).

13. With respect to claims 10, 20 and 29, Ikeda teaches all the elements of claims 9, 19 and 28, from which the claims depend respectively. Ikeda teaches: wherein the check rule involves at least one of: a single edge (see Figure 33, S86, wherein each Voronoi region includes a single pattern edge), a pair of neighboring edges, and edges within more than one layer of the IC design.

14. With respect to claim 11, Ikeda teaches all the elements of claim 1, from which the claim depends. Ikeda teaches: wherein each concave vertex of the shape is an interval (Figure 17 shows images of pattern with convex/concave contours, see Figure 17).

15. With respect to claim 31, Ikeda teaches all the elements of claim 30, from which the claim depends. Ikeda teaches: wherein the check rule is a width dependent spacing rule (see Figure 16, wherein searching/checking the spacing between the kernels CN2 and CN4 to the edge of a shape).

Allowable Subject Matter

16. Claims 3, 6, 16 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 6, 16 and 25, the prior art of record fails to teach:

wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and

wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

With respect to claim 3, the prior art made of record fails to teach:

wherein the core Voronoi diagram is generated based on a L(infinity) metric, and the assigning is based on a Euclidean metric, the L(infinity) metric defining a distance between two points in the shape as the maximum of a horizontal distance and a vertical distance between the two points.

Response to Arguments

18. Applicant's arguments filed 5/17/2007 have been fully considered but they are not persuasive. Examiner's response to arguments follow below:

19. Applicant asserts that Ikeda does not disclose "partitioning an edge of a shape in the IC design into a plurality of intervals". Examiner disagrees with this assertion.

20. Examiner points out that Ikeda teaches: partitioning (divided regions, paragraph [0184], also see divided edges of Figure 12) an edge (edges of a polygon, paragraph [0029], also see divided edges of Figure 12) of a shape (contour shape, paragraph [0016]) in the IC design (design data of the pattern, see Ikeda, claim 24) into a plurality of intervals (sequence of edge points, i.e. intervals, paragraph [0222]).

21. Applicant asserts that Ikeda does not have/has not extracted a pattern contour in an IC design. Examiner disagrees with this assertion.

22. Examiner points out that Ikeda teaches: an extracting a pattern contour (i.e. an extracting method of a pattern contour, see Abstract) in an IC design.

23. Applicant asserts that Ikeda does not teach "assigning at least one dimension to each interval". Examiner disagrees with this assertion.

24. Examiner points out that Ikeda teaches: assigning at least one dimension to each interval (a length Lij is imparted to each edge interval, paragraph [0170]).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER